PATENT APPLICATION

PATENT AND TRADEMARK OFFICE

BEFORE THE HONORABLE BOARD OF PATENT APPEALS AND INTERFERENCES

In re the Application of

Miki NAGANO

On Appeal from Group: 2623

Application No.: 09/743,863

Examiner: V. Kibler

Filed: January 17, 2001

Docket No.: 108103

For: IMAGE-PROCESING APPARATUS AND IMAGE-DISPLAYING APPARATUS

APPEAL BRIEF TRANSMITTAL

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Attached hereto is our Brief on Appeal in the above-identified application.

Also attached hereto is our Check No. 164030 in the amount of Five Hundred Dollars ($500.00) in payment of the Brief fee under 37 C.F.R. 1.17(c). In the event of any underpayment or overpayment, please debit or credit our Deposit Account No. 15-0461 as needed in order to effect proper filing of this Brief.

For the convenience of the Finance Division, two additional copies of this transmittal letter are attached.

Respectfully submitted,

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Date: February 25, 2005

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BRIEF ON APPEAL

Appeal from Group 2623

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TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The real party in interest is Seiko Epson Corporation, by way of an Assignment recorded in the U.S. Patent and Trademark Office at Reel 011500, Frame 0255.

II. STATEMENT OF RELATED APPEALS AND INTERFERENCES

There are no prior or pending appeals, interferences or judicial proceedings, known to Appellant, Appellant's representative, or the Assignee, that may be related to, or which will directly affect or be directly affected by or have a bearing upon, the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-13 stand rejected and are on appeal.

Claims 1-13 are pending.

No claims are allowed.

IV. STATUS OF AMENDMENTS

An Amendment After Final Rejection was filed on November 4, 2004. The Amendment After Final Rejection added new dependent claim 14, without amending any of claims 1-13.

In a December 3, 2004, Advisory Action, Examiner Kibler indicated that new claim 14 was not entered. Therefore, this Appeal proceeds with respect to claims 1-13.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The invention of independent claim 1 is directed to an image-processing apparatus that includes two or more image processing sections, such as on-screen display controllers (OSDCs) 120A, 120B and 120C (Figures 1 and 8; page 5, lines 11-17; page 10, lines 14-20; and page 11, lines 19-23). Data of two or more consecutive pixels are input to, and received by, the two or more respective image processing sections concurrently (page 9, lines 8-12; and page 10, lines 17-20). Also, the image processing sections concurrently process the respective pixels (page 9, lines 1-12).

The image processing apparatus also includes a control section, such as CPU 140, that controls the two or more image processing sections (Figures 1 and 7; page 4, lines 25-29; page 8, lines 16-31; and page 9, lines 13-20).

Each of the image processing sections (OSDC 120A, 120B and 120C) may be set to a master mode or a slave mode (page 9, lines 13-14). When in the master mode, an image processing section is permitted input access and/or output access to data bus DATA which is a CPU bus 142 in connection with the CPU 140 (Figures 5A and 5B; page 4, lines 25-29; and page 6, lines 23-33), whereby the image processing section in the master mode can communicate with the CPU 140 (control section). When in a slave mode, the image processing section is permitted only to receive data, and is inhibited from outputting data (Figures 5A and 5B; and page 7, lines 22-30). Among three image processing sections in an exemplary embodiment (OSDC 120A, 120B and 120C), one of them (for example, OSDC 120A) is set to the master mode, and the other two (for example, OSDC 120B and 120C) are set to the slave mode (page 10, lines 21-22).

Only an address space for a single OSDC is allocated in the I/O address space in the CPU 140, and the same I/O address is allocated for all the two or more image processing sections (Figure 6A, page 8, lines 6-9). When a request is commonly issued from the CPU 140

to the image processing sections, the CPU 140 concurrently controls all the image processing sections (page 8, lines 9-15; page 9, lines 14-20; and page 10, lines 20-29).

When the CPU 140 sends an image processing request to an image processing section in master mode (for example, OSDC 120A), each of the image processing sections (OSDC 120A, 120B and 120C) concurrently executes the same image processing (page 8, lines 6-15; page 9, lines 14-20; and page 10, lines 21-29).

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The following grounds of rejection are presented for review:

1) Claims 1-13 are rejected under 35 U.S.C. §102(e) over U.S. Patent No. 6,088,037 to Fukunaga et al. ("Fukunaga").

VII. ARGUMENT

The Examiner rejects claims 1-13 under 35 U.S.C. §102(e) as being anticipated by Fukunaga. However, the Examiner has improperly applied the law relating to anticipation. Proper application of the law demonstrates that anticipation has not been shown, and that the claimed invention is not anticipated by Fukunaga.

A. Fukunaga Does Not Disclose Each And Every Element Of Claim 1

1. The Office Action Impermissibly Picks and Chooses Features from Different Embodiments of Fukunaga, And Is Inconsistent With Its Assertion Regarding the Control Section

For example, in rejecting the claims, the Office Action asserts that Fukunaga discloses, at col. 6, lines 56-61, the recited element "a control section that controls the n image processing sections." The Office Action further asserts that Fukunaga discloses, at col. 15, lines 14-21, the recited element "commands are commonly given to the n image processing sections from the control section." However, the "control section" referred to in col. 6 is not the same "control section" referred to in col. 15. In fact, col. 6 and col. 15 refer to two separate embodiments.

In particular, the disclosure at col. 6, lines 56-61 of Fukunaga is directed to a first embodiment of Figs. 3 and 4. The disclosure at col. 6, lines 56-61 reads:

> Each rendering processor is provided with a signal 41 indicating a correspondence to a plane and a signal 42 enabling a synchronization for a data set or read operation via the bus 1 to the processor. The system is configured such that the signal 42 is outputted from **a control section of a master processor**. (Emphasis added.)

As quoted above, the "control section" in this context is "a control section of a master processor." This "control section" outputs a synchronization signal from the master processor. (See col. 14, lines 41-45.) Thus, the "control section" here is part of the master processor.

On the other hand, the disclosure at col. 15, lines 14-21 of Fukunaga is directed to a second embodiment of Figs. 13-15. The disclosure at col. 15, lines 14-21 reads:

> A command indicating a function of the rendering processor and data associated therewith sent from **the display control processor 1012** are set via the bus 1001 to registers in the processor element 1004-i. In the processor element 1004-i, as shown in FIG. 21 for example, the SL-MOD register 111 and the CSL-MOD register 113 constitute a two-stage configuration for the pipeline control, which enables the next command and data to be set even during an operation thereof. (Emphasis added.)

The "display control processor 1012" disclosed in the above-quoted context is shown in Fig. 14 as a separate element from the master processor 1004-1 (or any other rendering processor 1004-I). Thus, the "display control processor 1012" is not the same element as the "control section of a master processor."

In view of the above, the Office Action is improper on its face because it (1) is inconsistent in its assertions regarding the "control section" and (2) impermissibly picks and chooses features from different embodiments of Fukunaga.

Regarding the picking and choosing, see, for example, Akzo N.V. v. International Trade Commission, 808 F.2d 1471 (Fed. Cir. 1986), cert. denied, 107 Supreme Court 2490 (1987). In this case, it was attempted to invalidate a claim under §102 based on separate structures that were disclosed within a single patent. However, the Federal Circuit adopted an Administrative Law Judge (ALJ)'s decision, which "concluded in effect that the anticipatory reference must disclose in the prior art a thing substantially identical with the claimed invention" (Akzo at 1480) (emphasis added). The Court thus rejected "random picking and choosing" of elements, even if they are disclosed within a single reference. Yet, contrary to this holding, the Office Action picks and chooses from different embodiments.

2. Fukunaga Does Not Disclose "A First Operation Mode Allowing Data Communication With The Control Section, And A Second Operation Mode Allowing Only Reception From The Control Section"

The August 6, 2004 Final Rejection and the subsequent December 3, 2004 Advisory Action fail to prove that each and every claimed element is explicitly or inherently present in a device disclosed by Fukunaga. For example, the August 6, 2004 Final Rejection and the subsequent December 3, 2004 Advisory Action fail to prove that Fukunaga discloses the element "a first operation mode allowing data communication with the control section, and a second operation mode allowing only reception from the control section," recited in claim 1.

Fukunaga discloses a plurality of processor elements 1004-i, each of which receives commands from a display control processor 1012 during a rendering process. See col. 15, lines 14-21. Thus, each of the processor elements 1004-i is in an equal status with respect to its behavior with respect to the display control processor 1012.

Fukunaga discloses that 1004-1, the first of the processor elements 1004-i, is a "master" that outputs a synchronization signal so that the "other processor elements" are synchronized. See col. 14, lines 41-45. The only difference between the "master" and "the other processor elements," as disclosed in Fukunaga, is that the master outputs the synchronization signal. This difference does not constitute a difference in the way the processor elements 1004-i behave with respect to the display control processor 1012 (control section). Thus, Fukunaga does not disclose any difference between the master and the other processor elements regarding data communication with a control section.

In view of the above, Fukunaga does not disclose "a first operation mode allowing data communication with the control section, and a second operation mode allowing only reception from the control section," as recited in claim 1, and claims 2-13 depending therefrom.

3. The Examiner's Assertions Regarding "Master/Slave" Relationship Of Fukunaga Are Not Supported By Evidence Or Technical Reasoning

a. Prior Art's Disclosure Of a "Master/Slave" Relationship In the Context Of Generating Synchronization Signals Is Not Disclosure Of a "Master/Slave" Relationship In the Context Of Allowing Data Communication With a Control Section

The Office Action asserts that Fukunaga discloses a processor element being set as a master, thereby being set to one of a first operation mode allowing data communication with a control section. This assertion is incorrect.

The master/slave relationship disclosed in Fukunaga is narrowly limited within the context of generating a synchronization signal. See col. 14, lines 38-45. Fukunaga's "master/slave relationship" is irrelevant to data communication with a control section. Thus, by disclosing a master/slave relationship in the narrow context of generating a synchronization signal between processor elements, Fukunaga does not consequently disclose a master/relationship in the context of communicating data with a control section.

The argument that a disclosure of a master/slave relationship in the narrow context of generating a synchronization signal does not consequently disclose a master/relationship in the context of allowing data communication with a control section was presented in the November 4, 2004 Amendment After Final Rejection. However, the December 3, 2004 Advisory Action fails to adequately respond to this argument. The Advisory Action states that "the claim language does not exclude processor being synchronizers" (see the Advisory Action at page 3, lines 2-3), but this statement misses the mark. The issue regarding a processor element's behavior with respect to the control section is not addressed in the Advisory Action.

b. The Office Action Fails to Establish That a "Master/Slave Model Is Well-Known For Communication Protocol," Or Explain How Such Would Have Been Applied To Fukunaga

The Office Action asserts, without citing any reference, that a master/slave relationship is a well-known model for communication protocol. The November 4, 2004 Amendment After

Final Rejection requested that a reference be produced to demonstrate how an alleged "well-known" model for data communication protocol may be applied in Fukunaga's synchronization signal generation, so that Appellant can recognize and seek to counter the grounds for rejection. See *Chester v. Miller*, 15 USPQ2d 1333, 1337 (Fed. Cir. 1990).

However, the December 3, 2004 Advisory Action merely repeated that "master/slave relationship is a well-known model for communication protocol," and alleged that the model is applied in Fukunaga "as a rendering process." (See the Advisory Action at page 3, lines 5-7.) As discussed above, the master/slave relationship, as disclosed in Fukunaga, is limited to the context of generating synchronization signals. There is no disclosure in Fukunaga regarding a master/slave relationship in the context of a "rendering process."

In view of the above, the Examiner has not met her burden to demonstrate how this "well known model" is applied "as a rendering process."

c. The Examiner Has Not Proved That a "Master/Slave" Relationship In the Context Of Allowing Data Communication With a Control Section Is Inherent From a "Master/Slave" Relationship In the Context Of Generating Synchronization Signals

In order to be anticipatory under 35 U.S.C. §102, an applied reference must include each and every feature set forth in the claims that are being rejected over that reference. A prior art reference anticipates the subject matter of a claim when the reference discloses every feature of the claimed invention, either explicitly or inherently. See *Atlas Powder Co. v. IRECO Inc.*, 190 F.3d 1342, 1346, 51 USPQ2d 1943, 1945-46 (Fed. Cir. 1999); *In re Schreiber*, 128 F.3d 1473, 1477, 44 USPQ2d 1429, 1431 (Fed. Cir. 1997); *In re Paulsen*, 30 F.3d 1475, 1478,1479, 31 USPQ2d 1671, 1675 (Fed. Cir. 1994); *In re Spada*, 911 F.2d 705, 708, 15 USPQ2d 1655, 1657 (Fed. Cir. 1990); *Hazani v. Int'l Trade Comm'n*, 126 F.3d 1473, 1477, 44 USPQ2d 1358, 1361 (Fed. Cir. 1997); and *RCA Corp. v. Applied Digital Data Systems, Inc.*, 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984). It is well settled

that the burden of establishing anticipation resides with the Patent and Trademark Office (PTO). See *In re Piasecki*, 745 F.2d 1468, 223 USPQ 785, 788 (Fed. Cir. 1984).

The Office Action and the Advisory Action assert that, in a master/slave relationship, it is inherent that the slave has reception only. Notably, neither the Office Action nor the Advisory Action cite any authority supporting this assertion. Thus, the Examiner has not met her burden to establish inherency by explicit evidence or technical reasoning.

"To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference. . . . Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient'" (emphasis added). *In re Robertson*, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999); *In re Oelrich*, 666 F.2d 658, 581, 212 USPQ 323, 326 (CCPA 1981); and *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993).

In order to establish that, in a master/slave relationship, a slave inherently has reception only, the Examiner must prove the non-existence of any possibility in which the slave may transmit or output information. For example, the Examiner must prove, by explicit evidence or technical reasoning, that there is no possibility in which the slave may send information to the master when, for example, the master so requests. Appellant respectfully submits that, in fact, there are abundant examples in which slave devices transmit to a master device at some time.

The Examiner has produced no explicit evidence or technical reasoning to support her "inherency" assertion. Thus, the Examiner has not met her burden to demonstrate that, in a master/slave relationship, it is inherent that the slave has reception only.

B. Fukunaga Does Not Disclose Additional Features Claimed In Dependent Claims 3 and 6

The Office Action asserts that Fukunaga discloses, at col. 3, lines 30-37 and col. 14, lines 18-45, the additional elements recited in claims 3 and 6. This assertion is baseless.

Claims 3 and 6 recite, in pertinent part:

> each of the image processing sections including a mode-setting terminal that sets one of the first operation mode and the second operation mode, and one of the operation modes being set according to a mode-setting signal input to the mode-setting terminal.

On the other hand, the text at col. 3, lines 30-37 and col. 14, lines 18-45 of Fukunaga merely discloses that the rendering processors 1004-i may have a same structure in LSI (large scale integration), and that the processor element 1004-1 is set as the master to output the synchronization signal. The text at col. 3, lines 30-37 and col. 14, lines 18-45 of Fukunaga does not disclose when or how processor element 1004-1 is set as the master. In particular, nowhere in the text at col. 3, lines 30-37 and col. 14, lines 18-45 does Fukunaga disclose a mode-setting signal input to a mode-setting terminal, much less "one of the operation modes being set according to a mode-setting signal input to the mode-setting terminal," as recited in claims 3 and 6.

In view of the above, the Examiner fails to meet her burden in establishing that Fukunaga discloses each and every claimed element in claims 3 and 6.

C. Fukunaga Does Not Disclose Additional Features Claimed In Dependent Claims 4, 7 and 8

The Office Action asserts that Fukunaga discloses the additional elements recited in claims 4, 7 and 8. This assertion is baseless.

Claims 4, 7 and 8 recite, in pertinent part:

> wherein the image processing section set to the first operation mode can write the image-processing data, which is fed from the control section, to the memory, and in addition,

> can read out the image-processing data written in the memory; and
>
> wherein the image processing section set to the second operation mode can input the image-processing data read out by the image processing section set to the first operation mode from the memory.

The Office Action asserts that Fukunaga discloses, at col. 6, lines 45-47 and col. 13, line 64-67, "wherein the image processing section set to the first operation mode can write the image-processing data, which is fed from the control section, to the memory, and in addition, can read out the image-processing data written in the memory." However, Fukunaga, at col. 6, lines 45-47 and col. 13, line 64-67, merely discloses:

> Each processor is connected via the bus 2 to the frame memory 5, and all processors are connected to the display control processor 12 only via the bus 1.
> ...
> Each processor element is connected via the bus 1002 to the frame memory 1005, and all the processor elements are connected to the display processor 1012 only via the bus 1001.

As quoted above, the texts at col. 6, lines 45-47 and col. 13, line 64-67 of Fukunaga merely disclose that each processor or processor element is connected to a frame memory 5 (or a frame memory 1005). As specified in Fukunaga at col. 5, lines 57-65, the rendering processor 4 receives a command from a common memory 11 and only "effects a write control of the data in the frame memory 5." Nowhere does Fukunaga disclose writing image-processing data to the memory and reading out the image-processing data written in the memory. Thus, Fukunaga does not disclose "wherein the image processing section set to the first operation mode can write the image-processing data, which is fed from the control section, to the memory, and in addition, can read out the image-processing data written in the memory," as recited in claims 4, 7 and 8.

The Office Action also asserts that Fukunaga discloses, at col. 15, lines 14-21, "wherein the image processing section set to the second operation mode can input the image-processing

data read out by the image processing section set to the first operation mode from the memory." However, Fukunaga, at col. 15, lines 14-21, merely discloses:

> A command indicating a function of the rendering processor and data associated therewith sent from the display control processor 1012 are set via the bus 1001 to registers in the processor element 1004-i. In the processor element 1004-i, as shown in FIG. 21 for example, the SL-MOD register 111 and the CSL-MOD register 113 constitute a two-stage configuration for the pipeline control, which enables the next command and data to be set even during an operation thereof.

As quoted above, the texts at col. 15, lines 14-21 of Fukunaga merely disclose that the display control processor 1012 sends a command to the processor element 1004-i. These texts do not disclose inputting image-processing data that was read from the memory by another processor element. Thus, Fukunaga does not disclose "wherein the image processing section set to the second operation mode can input the image-processing data read out by the image processing section set to the first operation mode from the memory," as recited in claims 4, 7 and 8.

In view of the above, the Examiner fails to meet her burden in establishing that Fukunaga discloses each and every claimed element in claims 4, 7 and 8.

VIII. CONCLUSION

For any or all of the reasons discussed above, it is respectfully submitted that the rejection is in error and that claims 1-13 are in condition for allowance. Accordingly, Appellant respectfully requests this Honorable Board to reverse the rejection of claims 1-13.

Respectfully submitted,

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CLAIMS APPENDIX

CLAIMS INVOLVED IN THE APPEAL:

1. (Previously Presented) An image-processing apparatus, comprising:

n image processing sections which receive n consecutive pixel data items that are respectively input with the same timing and which respectively process the respective input pixel data items with the same timing, n representing an integer equal to at least "2"; and

a control section that controls the n image processing sections;

wherein each of the image processing sections are capable of being set to one of a first operation mode allowing data communication with the control section, and a second operation mode allowing only reception from the control section, one of the image processing sections is set to the first operation mode, and n−1 of the image processing sections are set to the second operation mode;

wherein commands are commonly given to the n image processing sections from the control section; and

wherein, when a command is given from the control section to the one of the image processing sections that is set to the first operation mode, the n image processing sections individually execute the same processing with the same timing.

2. (Previously Presented) The image-processing apparatus according to Claim 1, the n image processing sections being allocated in the same address space in address spaces that can be controlled by the control section.

3. (Previously Presented) The image-processing apparatus according to Claim 1, each of the image processing sections including a mode-setting terminal that sets one of the first operation mode and the second operation mode, and one of the operation modes being set according to a mode-setting signal input to the mode-setting terminal.

4. (Previously Presented) The image-processing apparatus according to Claim 1, further including a memory that stores image-processing data commonly used by the respective image processing sections,

wherein the image processing section set to the first operation mode can write the image-processing data, which is fed from the control section, to the memory, and in addition, can read out the image-processing data written in the memory; and

wherein the image processing section set to the second operation mode can input the image-processing data read out by the image processing section set to the first operation mode from the memory.

5. (Previously Presented) An image-displaying apparatus, comprising:

the image-processing apparatus according to Claim 1, and

an image-displaying section that displays images represented by video signals output from the image-processing apparatus.

6. (Previously Presented) The image-processing apparatus according to Claim 2, each of the image processing sections including a mode-setting terminal that sets one of the first operation mode and the second operation mode, and one of the operation modes being set according to a mode-setting signal input to the mode-setting terminal.

7. (Previously Presented) The image-processing apparatus according to Claim 2, further including a memory that stores image-processing data commonly used by the respective image processing sections,

wherein the image processing section set to the first operation mode can write the image-processing data, which is fed from the control section, to the memory, and in addition, can read out the image-processing data written in the memory; and

wherein the image processing section set to the second operation mode can input the image-processing data read out by the image processing section set to the first operation mode from the memory.

8. (Previously Presented) The image-processing apparatus according to Claim 3, further including a memory that stores image-processing data commonly used by the respective image processing sections,

wherein the image processing section set to the first operation mode can write the image-processing data, which is fed from the control section, to the memory, and in addition, can read out the image-processing data written in the memory; and

wherein the image processing section set to the second operation mode can input the image-processing data read out by the image processing section set to the first operation mode from the memory.

9. (Previously Presented) An image-displaying apparatus, comprising:

the image-processing apparatus according to Claim 2, and

an image displaying section that displays images represented by video signals output from the image-processing apparatus.

10. (Previously Presented) An image-displaying apparatus, comprising:

the image-processing apparatus according to Claim 3, and

an image displaying section that displays images represented by video signals output from the image-processing apparatus.

11. (Previously Presented) An image-displaying apparatus, comprising:

the image-processing apparatus according to Claim 4, and

an image displaying section that displays images represented by video signals output from the image-processing apparatus.

12. (Previously Presented) An image-processing apparatus according to claim 1, further comprising:

a CPU data bus,

the image processing section that is set to the first operation mode is permitted input access and/or output access to the CPU data bus, and the image processing sections that are set to the second operation mode are inhibited from outputting data to the CPU data bus.

13. (Previously Presented) An image-processing apparatus according to claim 1, each of the image processing sections including a mode control section that sets to one of the first operations mode and the second operation mode